AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions, and listings of claims in the application:

1. (Previously Presented) A system to communicate between a device and a controller, the system comprising:

a data line to communicate a data signal of a specific frequency from said device to said controller;

a clock line to communicate a clock signal of a specific frequency from said device to said controller;

an acknowledgement line to communicate an acknowledgement signal of a specific frequency from said controller to said device to verify receipt of said data signal; and

a guard line to communicate a guard signal from said device to said controller; wherein

the data signal comprises at least device information to be utilized by the controller;

the clock signal provides a timing reference, for transmission by the device and receipt by the controller, of the data signal;

said timing reference is verified through analysis of the guard signal in relation to the clock signal; and

data signal synchronization occurs through recognition of a bit pattern in the data signal.

2. (Previously Presented) The system of claim 1, wherein the acknowledgement signal frequency is equal to the clock signal frequency and the data signal frequency is twice the clock signal frequency.

3. (Original) The system of claim 1, wherein the device recognizes the receipt of the acknowledgement signal after sensing two consecutive binary transitions.

4. (Original) The system of claim 3, wherein the initial binary transition is 'high' to 'low' and the subsequent binary transition is 'low' to 'high'.

5. (Original) The system of claim 1, wherein the data signal synchronization occurs upon recognition of data signal maintenance at binary 'high' for five consecutive cycles of the clock signal.

6. (Original) The system of claim 1, wherein the guard signal operates at a specific phase and utilizes substantially the same waveform and period as the clock signal.

7. (Original) The system of claim 6, wherein the timing reference is verified by assuring that the guard signal is at an appropriate binary value given a specific activity of the clock signal.

8. (Original) The system of claim 7, wherein the timing reference is verified by assuring that when a transition of the clock signal from 'high' to 'low' is perceived, the guard signal is at a binary 'high', and when a transition of the clock signal from 'low' to 'high' is perceived, the guard signal is at a binary 'low'.

9. (Original) The system of claim 8, wherein timing reference is verified by assuring that the transition of the clock signal from 'low' to 'high' is recognized only when the previous

transition of the clock signal from 'high' to 'low' had a guard signal at a binary 'high'.

10. (Original) The system of claim 1, wherein the device information comprises a voltage identifier (VID), expressing the device's voltage requirement.

11. (Original) The system of claim 10, wherein the device voltage requirement is referenced by the controller to provide the device with an appropriate voltage supply.

12. (Original) The system of claim 11, wherein the device is a microprocessor and the controller is a voltage regulator.

13. (Original) The system of claim 11, further comprising a disable line to communicate a disable signal to the controller, wherein said disable signal is utilized to override normal operation of the controller and prevent communication between said device and controller.

14. (Currently Amended) A method to communicate between a device and a controller, comprising:

communicating, via a data line, a data signal of a specific frequency from said device to said controller;

communicating, via a clock line, a clock signal of a specific frequency from said device to said controller;

communicating, via a guard line, a guard signal from said device to said controller;

communicating, via an acknowledgement ~~line to communicate~~ line, an acknowledgement

signal of a specific frequency from said controller to said device to verify receipt of said data signal;

providing, within the data signal, at least device information to be utilized by the controller;

providing, by the clock signal, a timing reference, for transmission by the device and receipt by the controller, of the data signal;

verifying said timing reference through analysis of the guard signal in relation to the clock signal; and

synchronizing the data signal through recognition of a bit pattern in the data signal.

15. (Previously Presented) The method of claim 14, wherein the acknowledgement signal frequency is equal to the clock signal frequency and the data signal frequency is twice the clock signal frequency.

16. (Original) The method of claim 14, wherein the device recognizes the receipt of the acknowledgement signal after sensing two consecutive binary transitions.

17. (Original) The method of claim 16, wherein the initial binary transition is 'high' to 'low' and the subsequent binary transition is 'low' to 'high'.

18. (Original) The method of claim 14, wherein the data signal synchronization occurs upon recognition of data signal maintenance at binary 'high' for five consecutive cycles of the clock signal.

19. (Original) The method of claim 14, wherein the guard signal operates at a specific phase and utilizes substantially the same waveform and period as the clock signal.

20. (Original) The system of claim 19, wherein the timing reference is verified by assuring that the guard signal is at an appropriate binary value given a specific activity of the clock signal.

21. (Original) The system of claim 20, wherein the timing reference is verified by assuring that when a transition of the clock signal from 'high' to 'low' is perceived, the guard signal is at a binary 'high', and when a transition of the clock signal from 'low' to 'high' is perceived, the guard signal is at a binary 'low'.

22. (Original) The method of claim 21, wherein timing reference is verified by assuring that the transition of the clock signal from 'low' to 'high' is recognized only when the previous transition of the clock signal from 'high' to 'low' had a guard signal at a binary 'high'.

23. (Original) The method of claim 14, wherein the device information comprises a voltage identifier (VID), expressing the device's voltage requirement.

24. (Original) The method of claim 23, wherein the device voltage requirement is referenced by the controller to provide the device with an appropriate voltage supply.

25. (Original) The method of claim 24, wherein the device is a microprocessor and the controller is a voltage regulator.

26. (Original) The method of claim 24, further comprising a disable line to communicate a disable signal to the controller, wherein said disable signal is utilized to override normal operation of the controller and prevent communication between said device and controller.

27. (Original) A set of instructions residing in a storage medium, said set of instructions capable of being executed by a processor to communicate between a device and a controller, comprising:

communicating, via a data line, a data signal of a specific frequency from said device to said controller;

communicating, via a clock line, a clock signal of a specific frequency from said device to said controller;

communicating, via a guard line, a guard signal from said device to said controller;

communicating, via an acknowledgement line, an acknowledgement signal of a specific frequency from said controller to said device to verify receipt of said data signal;

providing, within the data signal, at least device information to be utilized by the controller;

providing, by the clock signal, a timing reference, for transmission by the device and receipt by the controller, of the data signal;

verifying said timing reference through analysis of the guard signal in relation to the clock signal; and

synchronizing the data signal through recognition of a bit pattern in the data signal.

28. (Previously Presented) The set of instructions of claim 27, wherein the acknowledgement signal frequency is equal to the clock signal frequency and the data signal frequency is twice the clock signal frequency; and wherein the data signal synchronization occurs upon recognition of data signal maintenance at binary 'high' for five consecutive cycles of the clock signal.

29. (Previously Presented) The set of instructions of claim 27, wherein the device recognizes the receipt of the acknowledgement signal after sensing an initial binary transition from 'high' to 'low' and a subsequent binary transition from 'low' to 'high'; and wherein the timing reference is verified by assuring that, upon sampling, the guard signal is a binary 'low' when the clock signal is a binary 'high' and that the guard signal is a binary 'high' when the clock signal is a binary 'low'.

30. (Previously Presented) The set of instructions of claim 27, wherein the device information comprises a device voltage requirement to be referenced by the controller for provision of an appropriate voltage supply to the device and wherein the device is a microprocessor and the controller is a voltage regulator.